WHAT IS CLAIMED IS:

1. A surface treatment method for a compound semiconductor layer, the compound semiconductor layer including nitrogen, the method including a nitrogen plasma treatment step to recover from damage due to nitrogen vacancies arising in a surface of the compound semiconductor layer.

2. The surface treatment method of claim 1, wherein the nitrogen plasma treatment step is performed by inductively coupled plasma reactive ion etching.

3. The surface treatment method of claim 1, wherein the nitrogen plasma treatment step is performed by non-etching exposure to nitrogen plasma.

4. The surface treatment method of claim 1, wherein the treated surface of the compound semiconductor layer is rinsed with pure water after the nitrogen plasma treatment step.

5. A surface treatment method for a compound semiconductor layer, the compound semiconductor layer being a compound semiconductor multilayer comprising a first compound semiconductor layer including nitrogen and a second compound semiconductor layer formed on and differing in composition from the first compound semiconductor layer, the method including:

removing part of the second compound semiconductor layer by dry etching to partially expose a surface of the first compound semiconductor layer; and

performing a nitrogen plasma treatment step to recover from damage due to nitrogen vacancies arising in the exposed surface of the first compound semiconductor layer.

6. The surface treatment method of claim 5, wherein the first compound semiconductor layer comprises aluminum gallium nitride ($Al_xGa_{1-x}N$, $0 < x < 1$) and the second compound semiconductor layer comprises gallium nitride (GaN).

7. The surface treatment method of claim 5, wherein the nitrogen plasma treatment step is performed by inductively coupled plasma reactive ion etching.

8. The surface treatment method of claim 5, wherein the nitrogen plasma treatment step is performed by non-etching exposure to nitrogen plasma.

9. The surface treatment method of claim 5, wherein the treated surface of the first compound semiconductor layer is rinsed with pure water after the nitrogen plasma treatment step.

10. A method of fabrication of a semiconductor device, the method comprising:

forming a compound semiconductor multilayer on a substrate, the compound semiconductor multilayer having a first compound semiconductor layer including nitrogen and a second compound semiconductor layer formed on and differing in composition from the first compound semiconductor layer;

forming a first main electrode and a second main electrode on the second compound semiconductor layer, the first and second main electrodes being mutually separated by a certain distance;

removing an area of the second compound semiconductor layer between the first main electrode and the second main electrode by dry etching to expose a surface of the first compound semiconductor layer;

annealing the partially exposed first compound semiconductor layer;

treating at least part of the exposed surface area of the first compound semiconductor layer with nitrogen plasma; and

forming a gate electrode on said part of the exposed surface area of the first compound semiconductor layer.

11. The method of fabrication of a semiconductor device of claim 10, wherein the first compound semiconductor layer comprises aluminum gallium nitride ($Al_xGa_{1-x}N$, $0 < x < 1$) and the second compound semiconductor layer comprises gallium nitride (GaN).

12. The method of fabrication of a semiconductor device of claim 10, wherein the treatment with nitrogen plasma is performed by inductively coupled plasma reactive ion etching.

13. The method of fabrication of a semiconductor device of claim 10, wherein the nitrogen plasma treatment step is performed by non-etching exposure to nitrogen plasma.

14. The method of fabrication of a semiconductor device of claim 10, further comprising rinsing the treated surface of the first compound semiconductor layer with pure water after the nitrogen plasma treatment step.

15. The method of fabrication of a semiconductor device of claim 10, wherein the semiconductor device is a high electron mobility transistor.